Power Efficiency in a Partially Reconfigurable Multiprocessor System

Raymond J. Weber
ECE Department
Montana State University
Bozeman, Montana 59717
raymond.weber@
msu.montana.edu

Justin A. Hogan
ECE Department
Montana State University
Bozeman, Montana 59717
justin.hogan@
msu.montana.edu

Brock J. Lameres
ECE Department
Montana State University
Bozeman, Montana 59717
lameres@
ece.montana.edu

Todd Kaiser
ECE Department
Montana State University
Bozeman, Montana 59717
tjkaiser@
ece.montana.edu

ABSTRACT

This paper describes the benchmarking of an FPGA-based computing system that uses partially reconfigurable tiles for real-time allocation of hardware resources. This system was developed for use in the aerospace industry in order to provide redundancy for fault mitigation and real-time hardware reallocation to reduce mass associated with separate functional systems. In this paper, we present the results of performance studies on our Xilinx Virtex-6 platform using the Dhrystone, LINPACK and NAS-Kernel benchmarks. We further present the impact on power consumption as processors and hardware accelerators are brought online to increase performance.

Categories and Subject Descriptors

C.4 [**Performance of Systems**]: Performance attributes; J.2 [**Physical Sciences and Engineering**]: Aerospace

Keywords

FPGA, Partial Reconfiguration, Benchmarking

1. INTRODUCTION

In partially reconfigurable computation most of the research attention has been focused on the performance and logic space improvements that are yielded by using the technique with less attention paid to the power enhancements for low power systems. In this research we have implemented a nine-tile partially reconfigurable system consisting of microprocessors and hardware accelerator tiles andmeasured power consumption versus the benchmarking performance.

2. TECHNIQUE AND RESULTS

For our system design, we seek to maximize system performance while minimizing power to favor system implementation in space based applications. We have implemented Whetstone, Dhrystone and LINPACK benchmarks to measure performance on single microprocessor tiles and single microprocessor + hardware accelerator systems. We have determined that NAS benchmarking kernels fit well with our multiprocessor system and have chosen to implement the EP kernel in this system.

We use a Microblaze microprocessor on the Spartan-6 FPGA for system control. This Microblaze is tasked with programming, monitoring, and activating/deactivating tiles on the Virtex-6 FPGA as well as communicating with a user PC. This arrangement leaves the Virtex-6 free to be used entirely by computational tiles. The lower power of the Spartan-6 makes it the ideal fabric to be constantly running from the overall power consumption standpoint.

We are able to dynamically activate and deactivate tiles on the Virtex-6 chip while monitoring the power consumption. Tracking power consumption versus benchmarking scores achieved by the system allows us to view the effects that hardware accelerators have, not only on performance, but also on the amount of power consumed by the system. This will allow for us to develop higher efficiency systems and identify trade-offs between additional generic microprocessors and specialized hardware accelerators.

We are running multiple benchmarking routines to evaluate the different applications of the chip. Testing integer, single precision and double precision floats, as well as matrix manipulations, extends the generality of this study making it useful for both PR and static FPGA designs. This enables evaluation on the trade-offs between hardware and software solutions with respect to the power requirements of the system.

3. CONCLUSION

The testing with the benchmarking tools to date has shown that our system is capable of running the benchmarking tools, and the monitoring capabilities of our hardware are able to record the power consumption changes in real-time as additional tiles are programmed and activated.

ICS'13, June 10–14, 2013, Eugene, Oregon, USA.
ACM 978-1-4503-2130-3/13/06.