# 3D/SiP Advanced Packaging Symposium

**Session II: Wafer Level Integration & Processing**
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# Off-Chip Coaxial to Coplanar Transition Using a MEMS Trench

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# Problem Statement

- **System Performance in VLSI Designs is Limited by Package Interconnect**
  - **1) Signal Path Reflections**
    - **- Unwanted Switching**
    - **- Edge Speed Degradation**
  - **2) Signal Coupling**
    - **- NE/FE Cross-talk**
    - **- Power Supply Droop**
    - **- Ground Bounce|**
- **On-Chip Performance is outpacing Off-Chip interconnect**
  - **1) Emerging problem of getting high speed signals from chip-to-chip**
  - **2) This problem will continue as transistors keep getting faster**

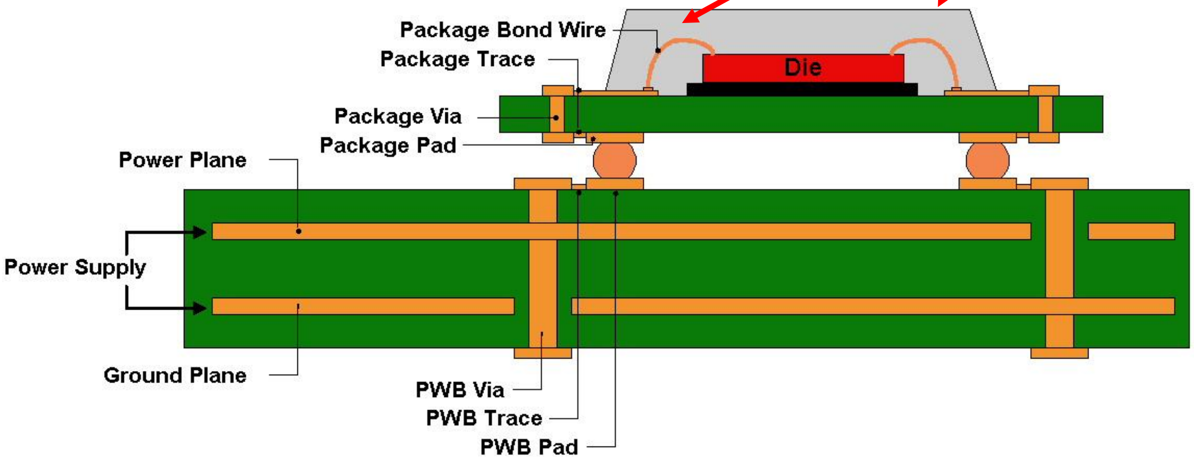
# Why is packaging limiting performance?

- **Today's Package Interconnect Looks Inductive**

  - Long interconnect paths
  - Large return loops

**Wire Bond Inductance (~2.8nH)**

$$L = \frac{\Phi}{I}$$



- **Today's Package Impedance is *Not Controlled* or *Shielded***

# The Trend Toward *System in Package (SiP)*

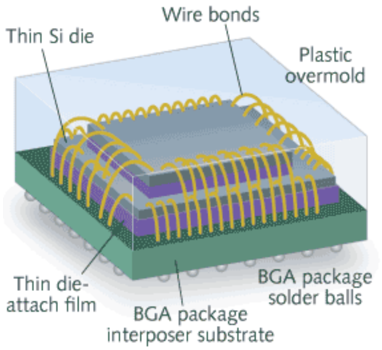
- **Moving more functionality on package reduces the amount of times a signal needs to traverse level 2 interconnect** ***(package-to-PCB)***

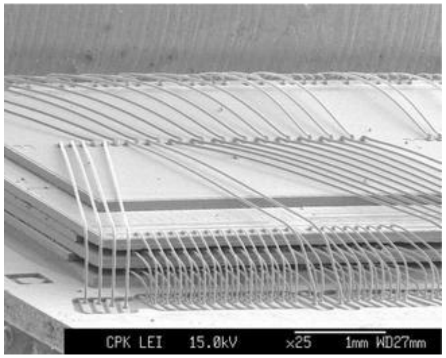
- **Integrating functionality onto a single IC has limitations:**

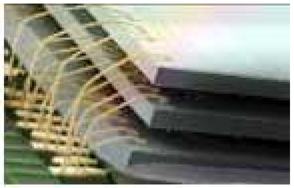
  - Reduced yield, suboptimal material selection (CMOS vs. GaAs vs. SiGe)

- **Integrating multiple die onto the same package with wire bonds is an optimal balance**

- **However, we're back to the problem of <u>unshielded,</u> <u>uncontrolled</u> wire bonds**







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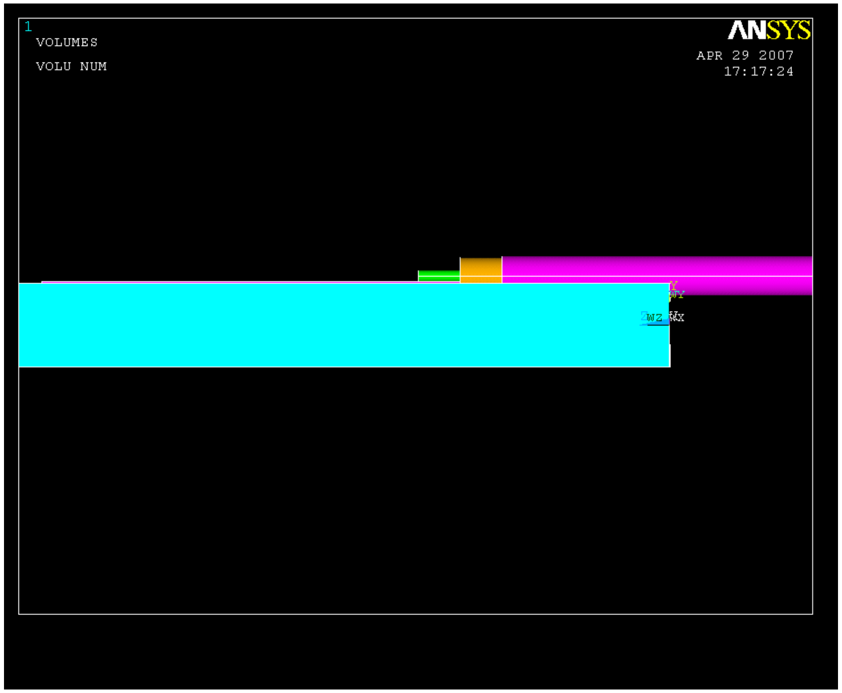
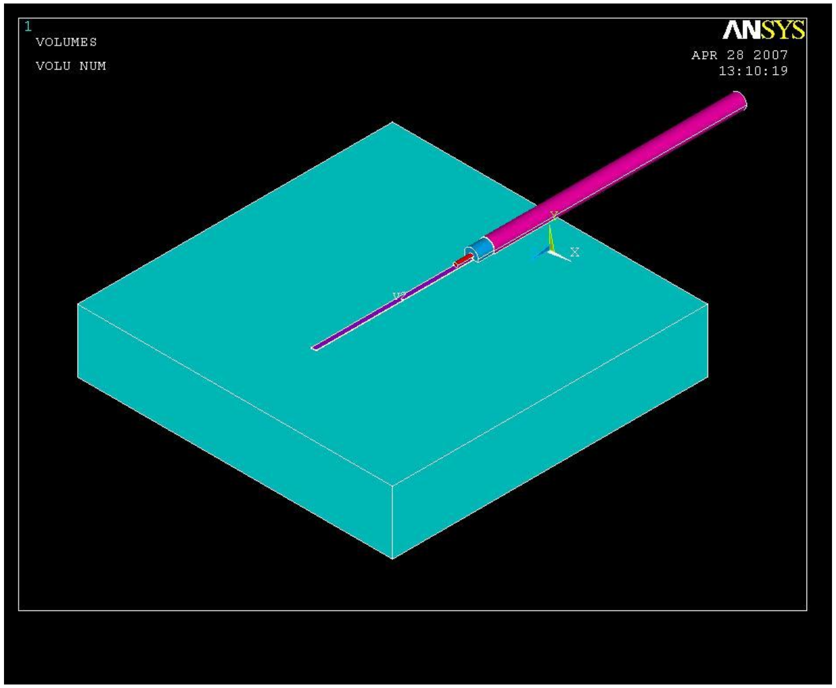
# Proposed Solution – *A New Chip-to-Chip Interconnect Technology*

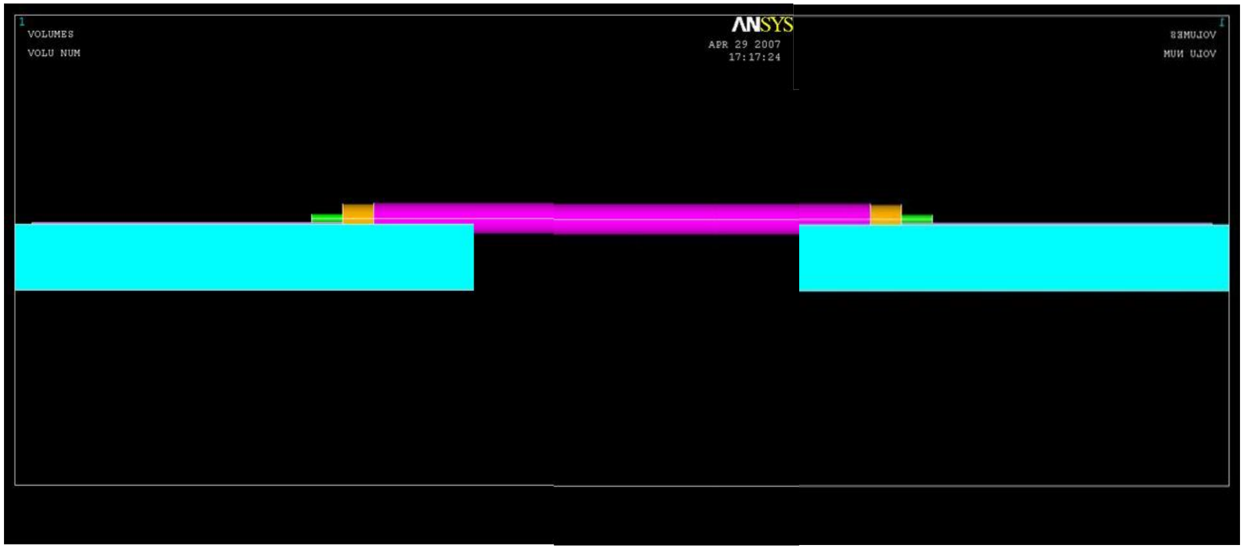
- **Off-Chip Coaxial Launch**
  - - Exploit Advances in MEMS process technology
  - - Target System in Package (SiP) applications





# Proposed Solution – *A New Chip-to-Chip Interconnect Technology*

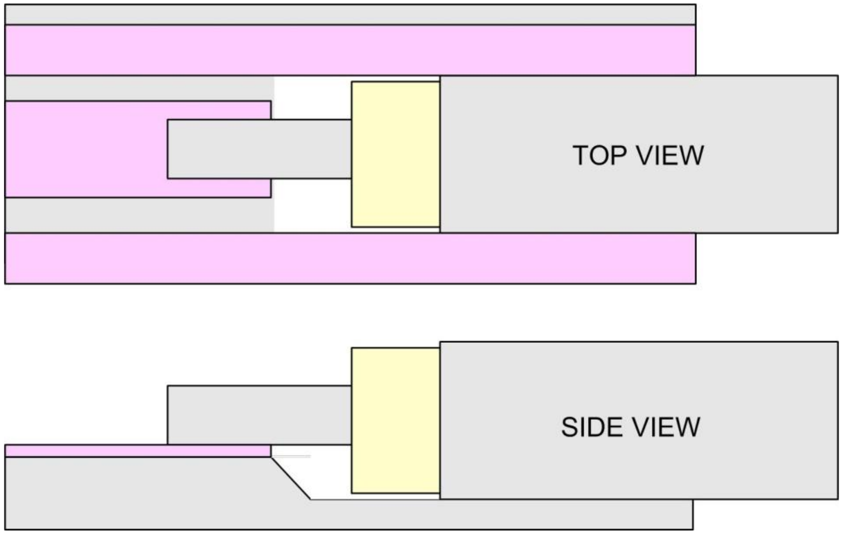
- **Application**
  - High speed chip-to-chip signals require controlled impedance and shielding
  - Additional process step converts perimeter wire-bond pads to coaxial launch.



  - Step 1: Design, Model, and Fabricate interconnection between side-by-side die
  - Step 2: Investigate Vertically Stacked Die Interconnect

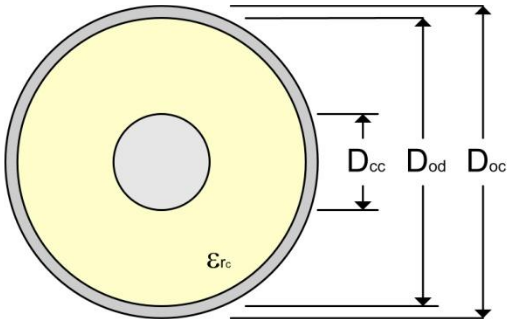
# Proposed Solution – *A New Chip-to-Chip Interconnect Technology*

- **Processing**
    - Etch a trench into the Silicon substrate to hold the coaxial cable
    - The center conductor is connected to a signal trace on-chip
    - A coplanar transmission line is used on-chip to provide connection to the signal and to the coaxial ground shield.



# Coaxial to Coplanar Launch

## Geometric Dependencies - Coaxial Line

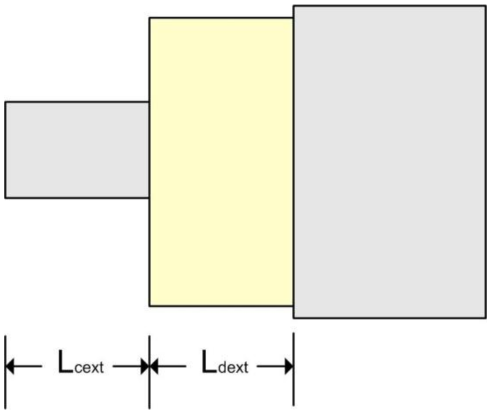


- The coax outer diameter is the key dimension

- Our design evaluations Semi-Rigid Coax's from *Micro-Coax* (UT-013, UT-020)

- 50Ω impedance requirement sets coaxial dimensions

- Extension diameters dictated by mechanical reliability

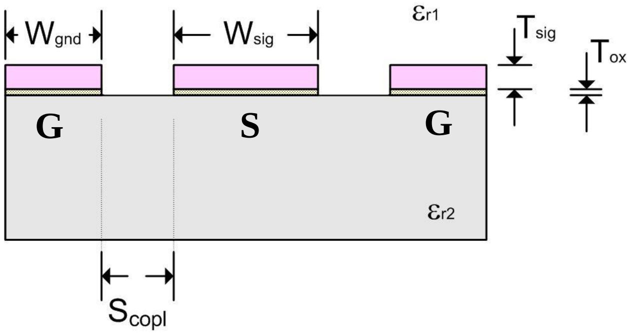


$$Z_{0_{coax}} = \frac{138}{\varepsilon_r} \cdot \log\left(\frac{D_{od}}{D_{cc}}\right)$$

# Coaxial to Coplanar Launch

## Geometric Dependencies - Coplanar Line

- The ground separation is dictated by the outer diameter of the coaxial line



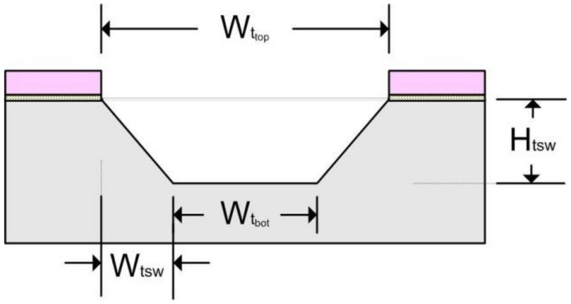
- 50Ω impedance set by material properties & signal trace width

NOTE: On-Chip Coplanar Transmission Line has:

1) Imaginary Impedance due to Lossy Semiconductor Material
2) Potential for higher-order modes in addition to TEM

# Coaxial to Coplanar Launch

## Geometric Dependencies - Trench



- The trench must be wide enough to accept the coaxial outer diameter

- The depth must place the coaxial center conductor on top of the coplanar signal trace

- Using inscribed octagonal geometries sets width of trench

- Anisotropic etch rate dictates angle of trench sidewall.

$$W_{t_{bot}} = D_{oc} \cdot \tan(22.5)$$

$$H_{tsw} = \frac{H_t}{\sin(45)}$$

$$W_{tsw} = \frac{H_t}{\tan(45)}$$

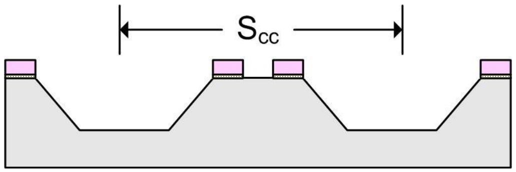
$$W_{t_{top}} = W_{t_{bot}} + 2 \cdot W_{tsw}$$

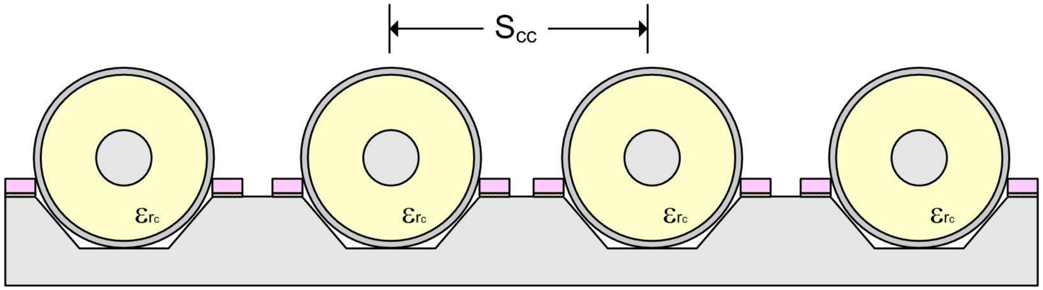
$$H_t = \left(\frac{D_{oc}}{2}\right) - \left(\frac{D_{cc}}{2}\right) - T_{ms}$$

# Coaxial to Coplanar Launch

## Geometric Dependencies – Channel Spacing

- Spacing of adjacent trenches must accommodate coax protrusion



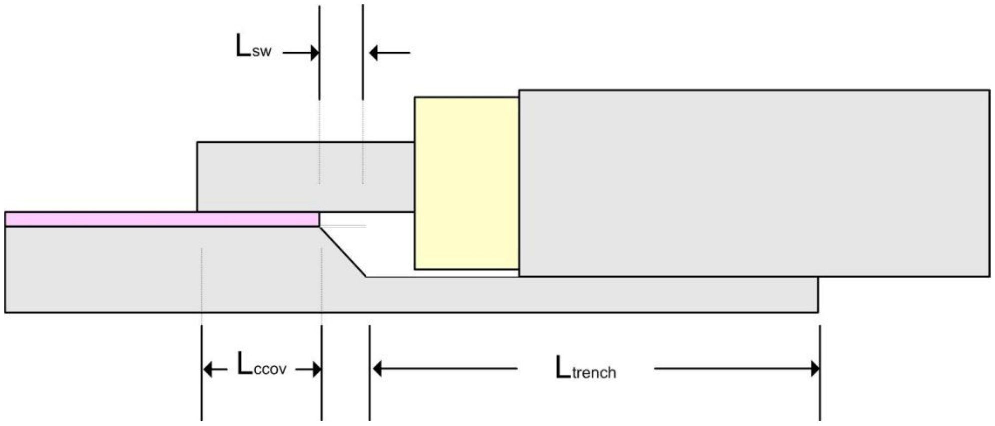


# Coaxial to Coplanar Launch

## Geometric Dependencies – Transition Region

- Length of sidewall dictated by anisotropic etch rate.

- Overlapping lengths dictated by mechanical reliability

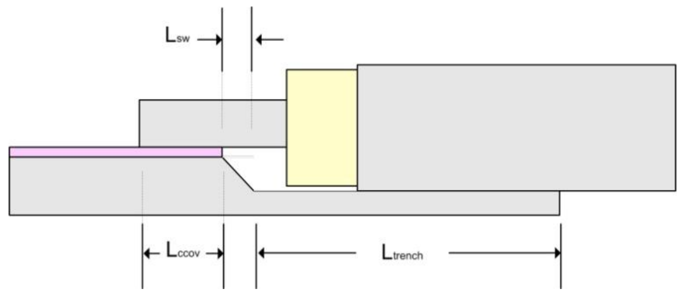


# Coaxial to Coplanar Launch

## Summary of Dimensions

- 2 Micro-Coax's are evaluated (UT-013, UT-020)

- Each coax size influences the trench and coplanar transmission line dimensions



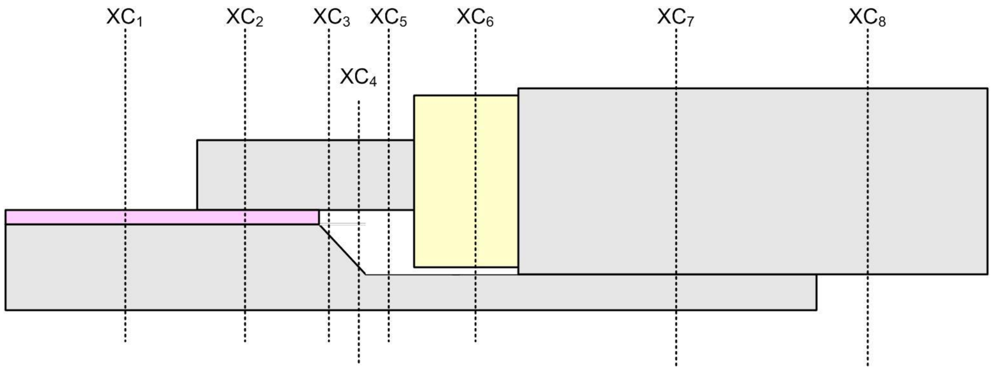
| Region | Parameter | Units | Coaxial Line | |
|---|---|---|---|---|
| | | | UT-013 | UT-020 |
| Coaxial Structure | $D_{oc}$ | μm | 330 | 584 |
| | $D_{od}$ | μm | 254 | 419 |
| | $D_{cc}$ | μm | 79 | 127 |
| Coplanar Structure | $T_{sig}$ | μm | 1 | 1 |
| | $T_{ox}$ | μm | 0.8 | 0.8 |
| | $W_{sig}$ | μm | 239 | 446 |
| | $W_{gnd}$ | μm | 100 | 100 |
| | $S_{copl}$ | μm | 55 | 90 |
| | $S_{ss}$ | μm | 634 | 916 |
| Trench Structure | $W_{ttop}$ | μm | 349 | 626 |
| | $W_{tbot}$ | μm | 150 | 228 |
| | $W_{tsw}$ | μm | 100 | 169 |
| | $H_{tsw}$ | μm | 141 | 239 |
| Transition Region | $L_{trench}$ | μm | 1100 | 1170 |
| | $L_{dext}$ | μm | 500 | 500 |
| | $L_{sw}$ | μm | 100 | 170 |
| | $L_{cext}$ | μm | 1000 | 1000 |
| | $L_{ccov}$ | μm | 900 | 831 |

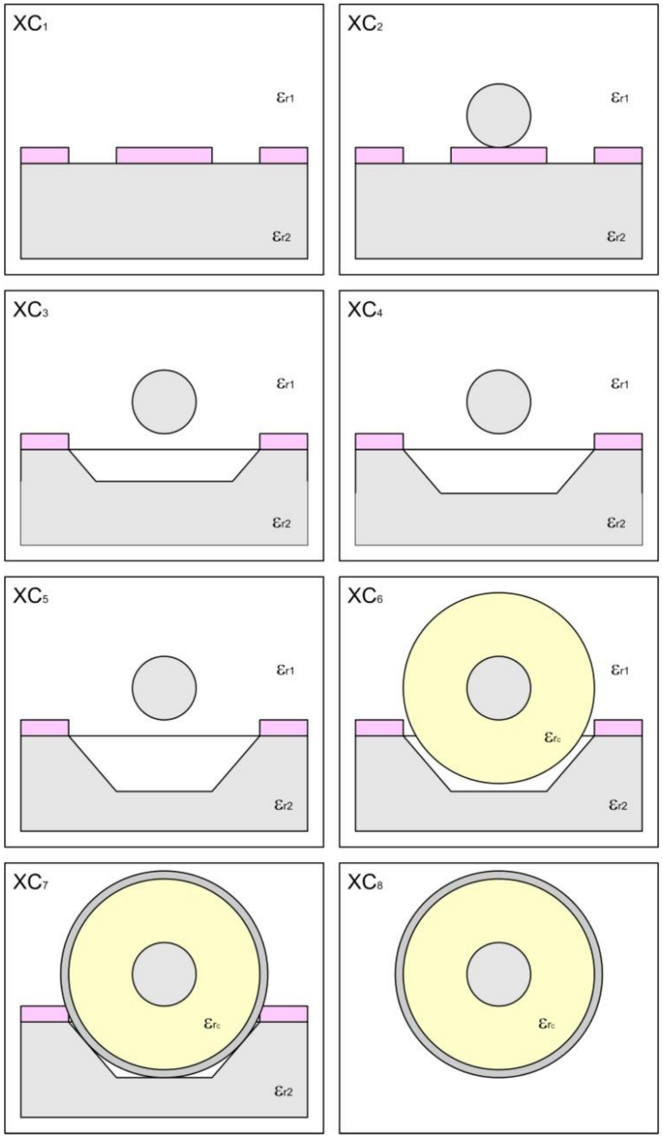
# Coaxial to Coplanar Launch

## Impedance Discontinuities

- Between the coax and coplanar T-lines, there are regions of impedance discontinuities

- These add reflections and risetime degradation between the two *ideal* transmission line structures (i.e., the coaxial and coplanar lines)





# Modeling Approach

## EM Field Solvers

- Due to the complexity of the structure, a field solver is used to extract the characteristic impedance ($Z_0$) and propagation constant (g)

- $Z_0$ and g are complex for signal propagation on the integrated circuit due to the use of a semiconductor substrate material.

- $Z_0$ is real inside of the coaxial transmission line

- We used *Electromagnetic Design Systems (EMDS)* from *Agilent Technologies* to perform 2D and 3D field simulations

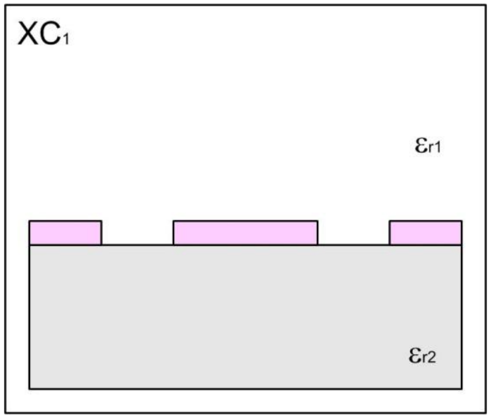
# Modeling Approach

## Our Approach

1) Extract $Z_0$ and g for each different Cross-Section within the transition using a 2D simulation

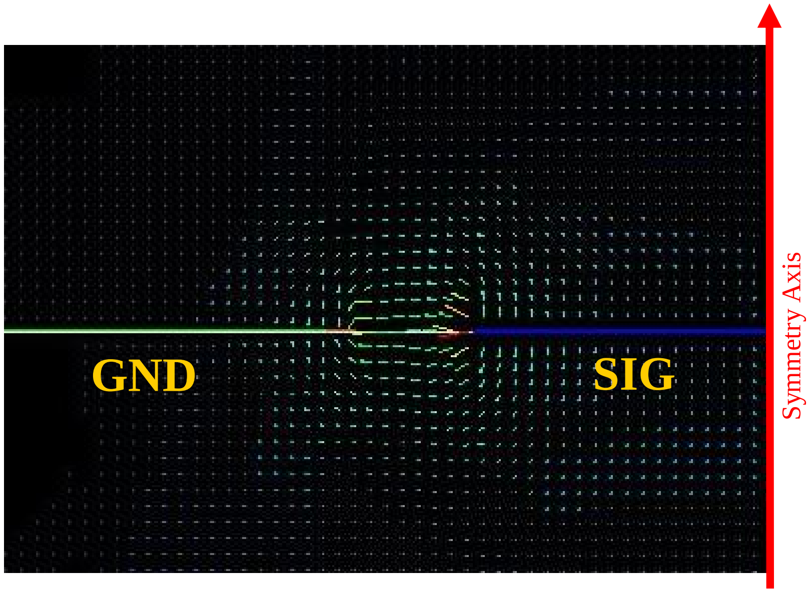
2) Import parameters into SPICE to perform transient simulations on the structures ability to transmit high speed signals

# Modeling Results (XC1)

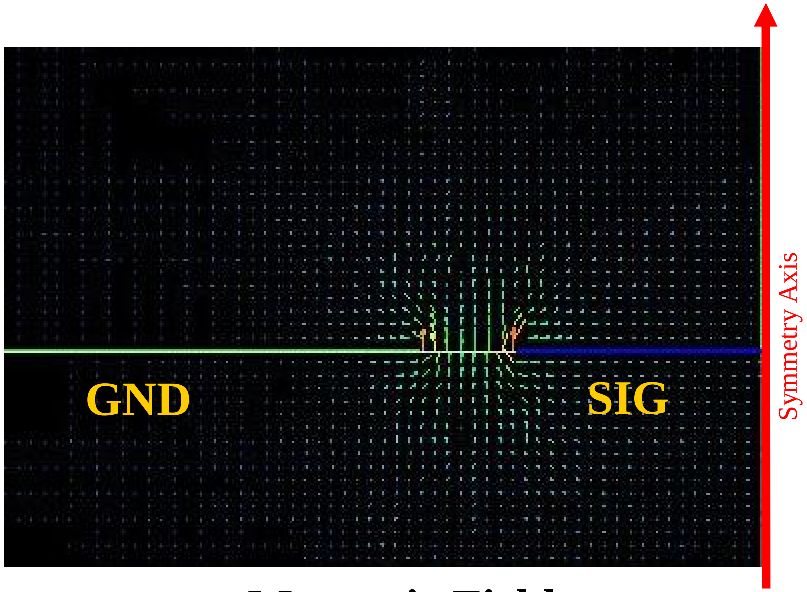


**Field Solder Results**

$$Z_0 = 52 + j26$$
$$\gamma = 305 + j615$$



**Electric Fields**

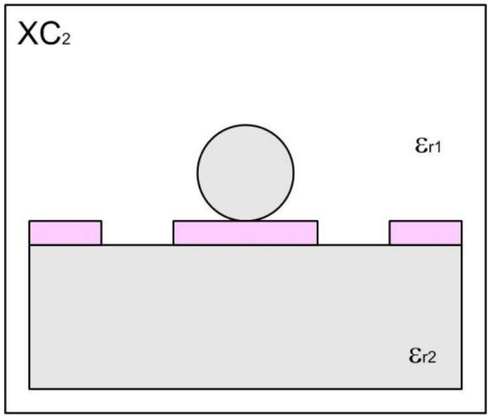


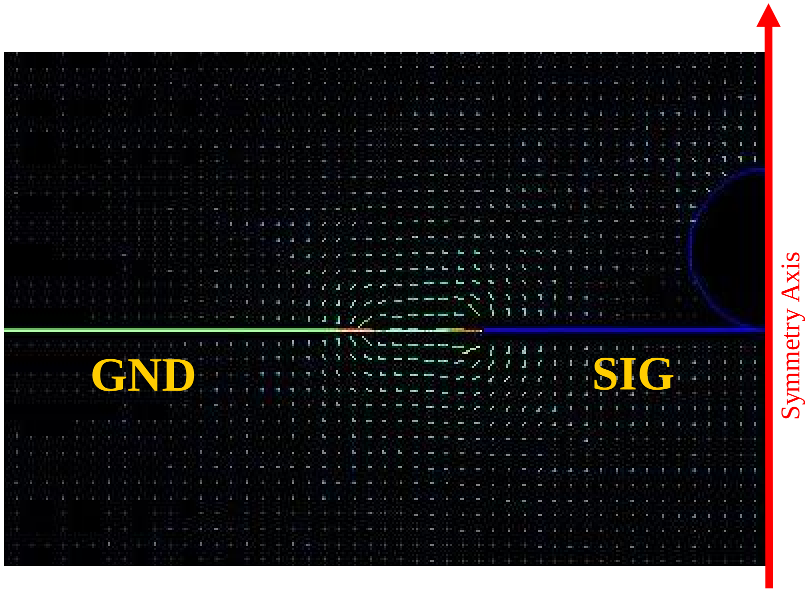
**Magnetic Fields**

# Modeling Results (XC2)

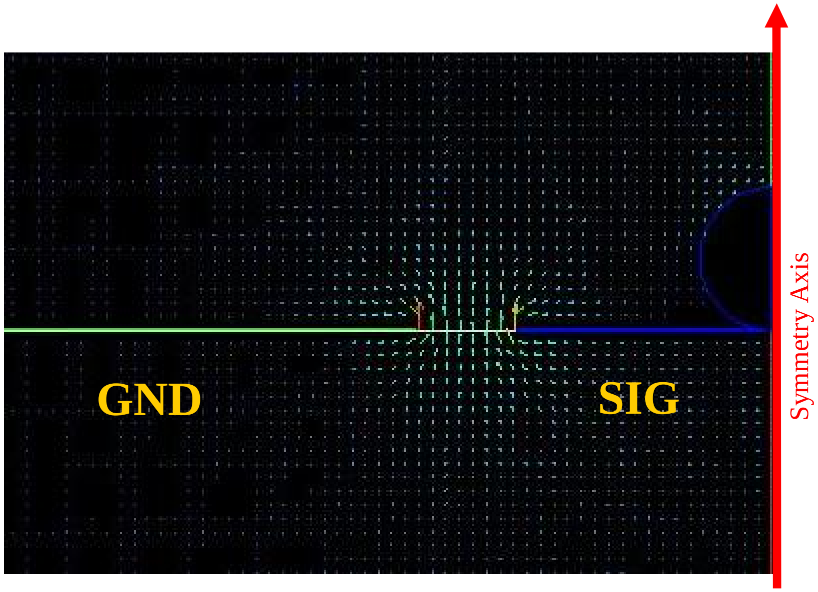
**Field Solder Results**

$$Z_0 = 50 + j25$$
$$g = 299 + j604$$



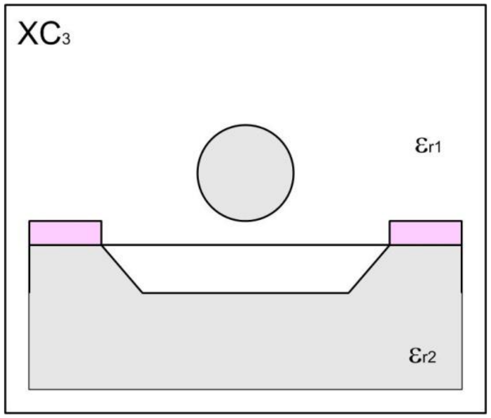


Electric Fields



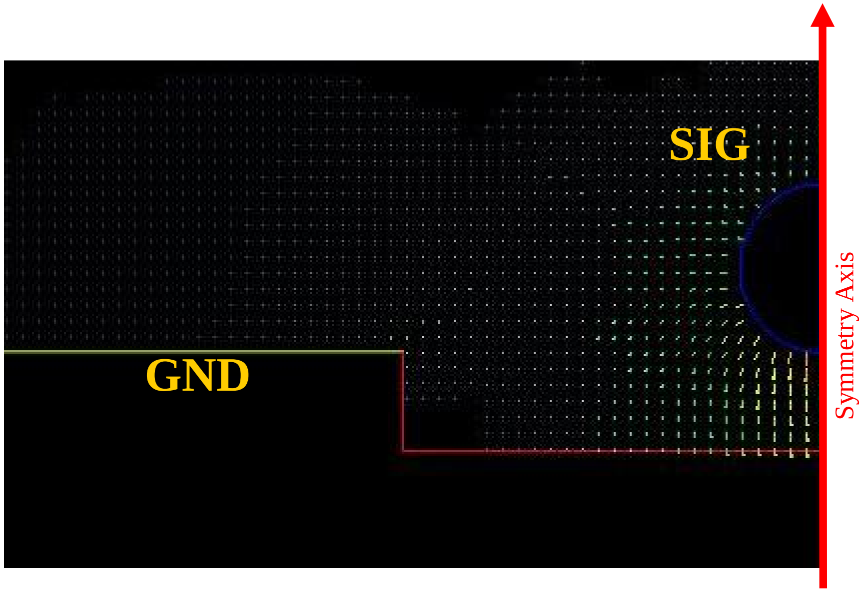
Magnetic Fields

# Modeling Results (XC3)

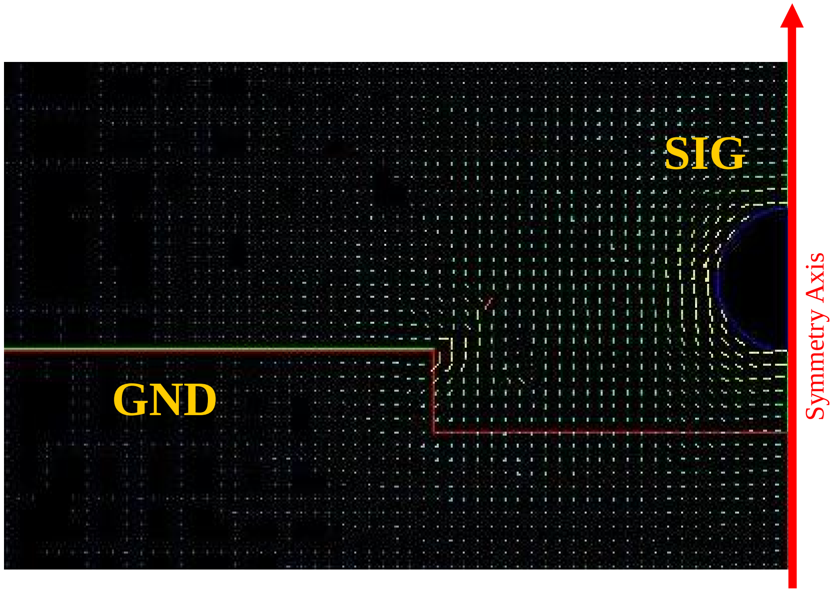


## Field Solder Results

$$Z_0 = 114 + j3$$
$$g = 10 + j269$$

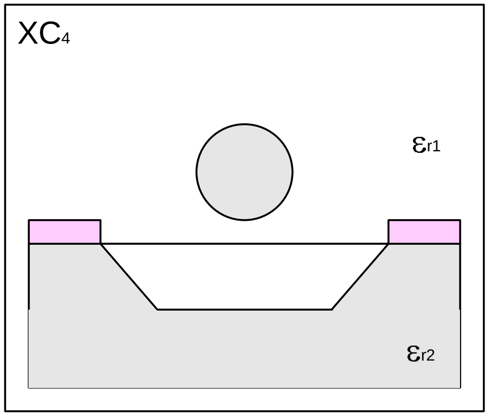


**Electric Fields**



**Magnetic Fields**

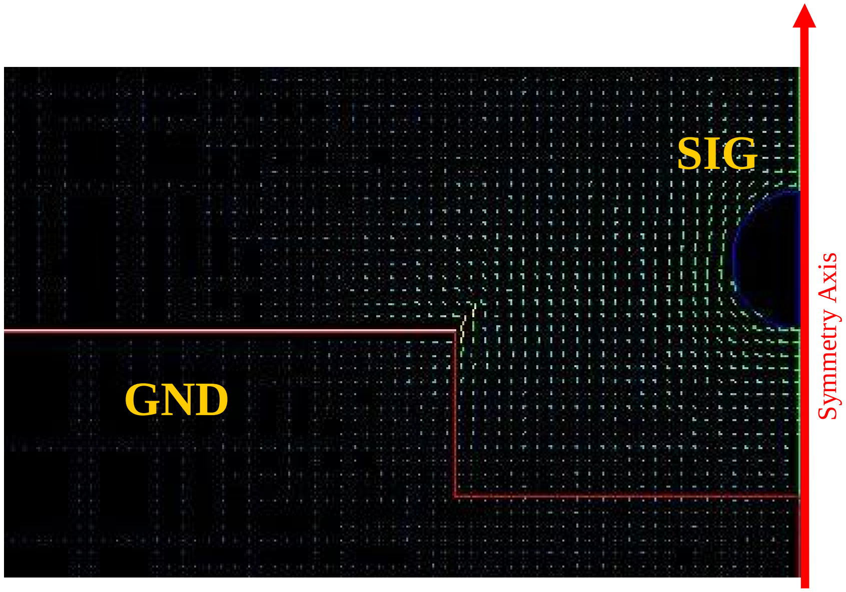
# Modeling Results (XC4)



**Field Solver Results**

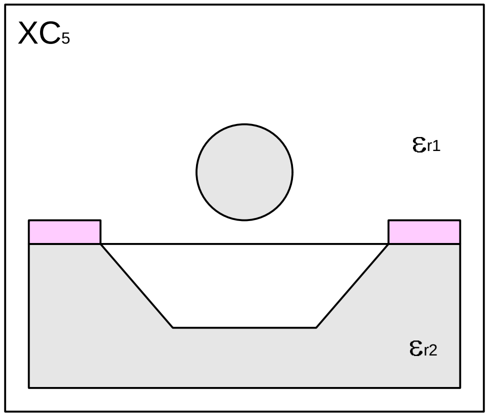
$$Z_0 = 128 + j1$$
$$g = 4 + j239$$

Electric Fields



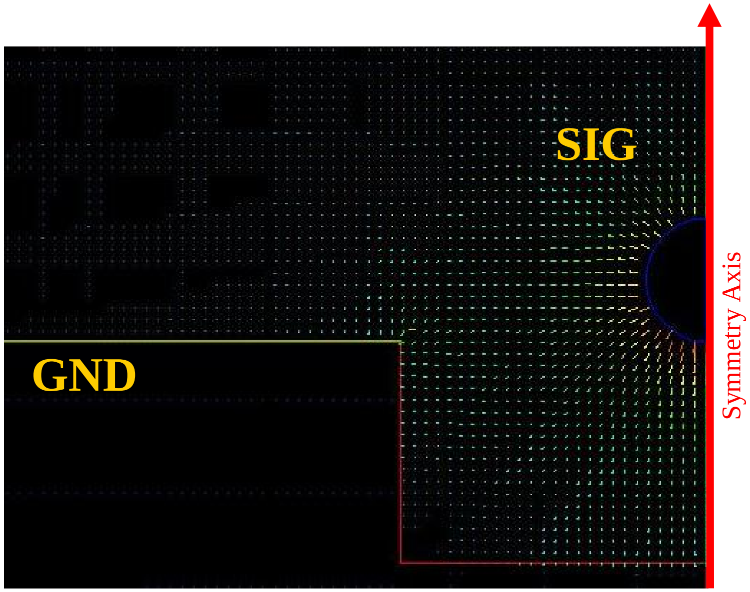
Magnetic Fields

# Modeling Results (XC5)

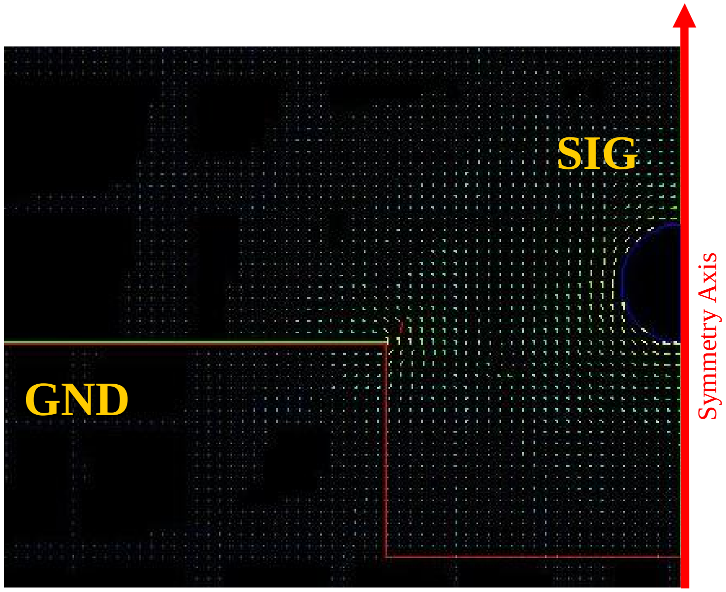


## Field Solver Results

$$Z_0 = 134 + j1$$
$$g = 3 + j229$$

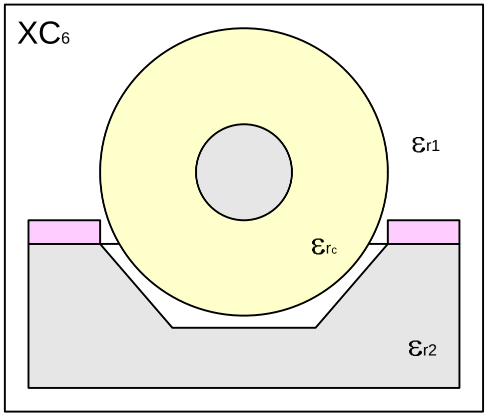


**Electric Fields**



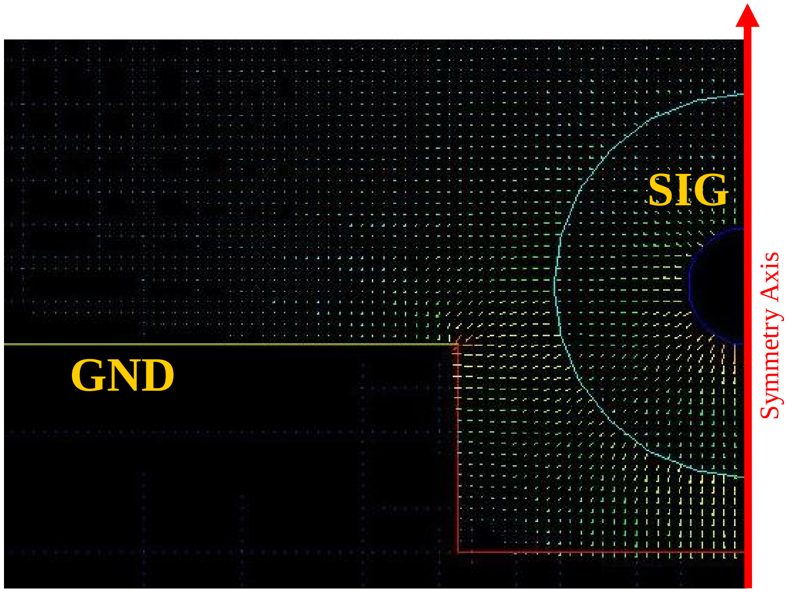
**Magnetic Fields**

# Modeling Results (XC6)

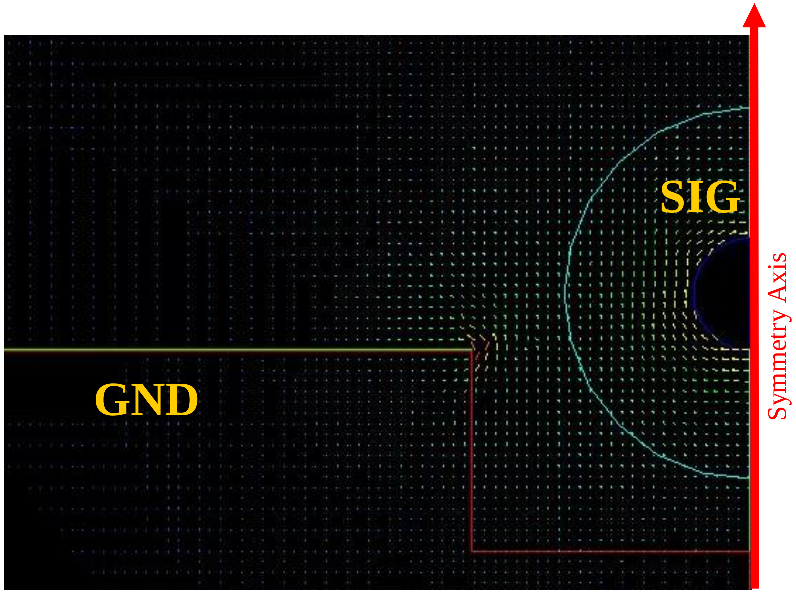


**Field Solver Results**

$$Z_0 = 111 + j1$$
$$g = 5 + j276$$

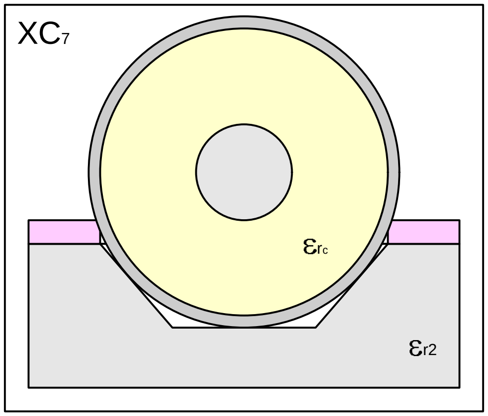


Electric Fields



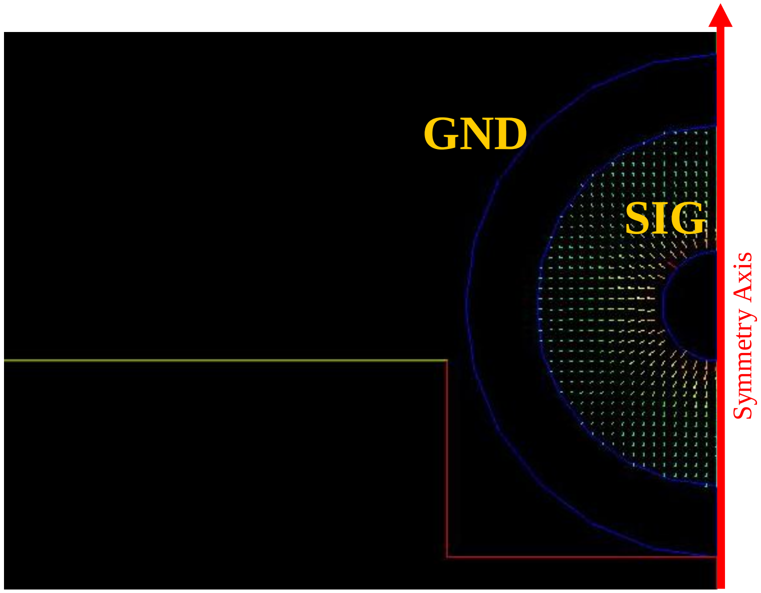
Magnetic Fields

# Modeling Results (XC7)

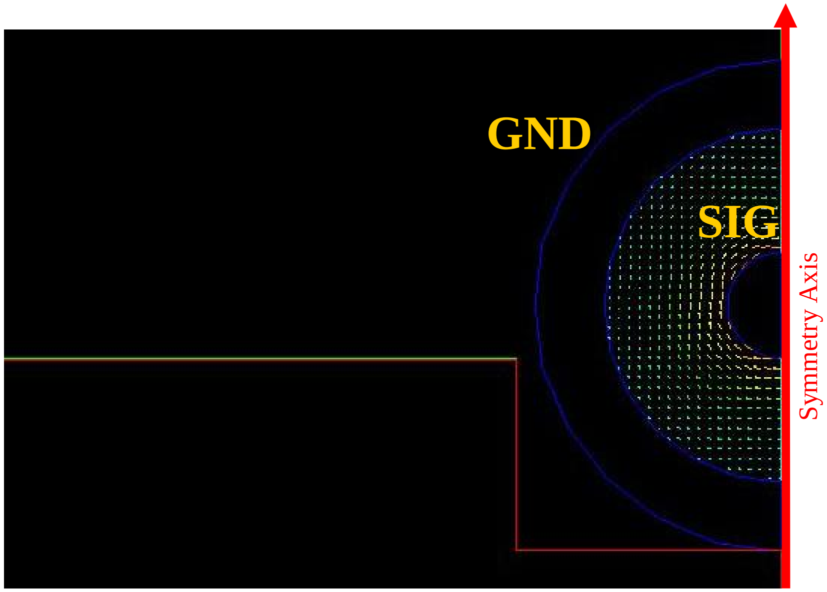


## Field Solver Results

$$Z_0 = 50 + j0$$
$$g = 0 + j296$$

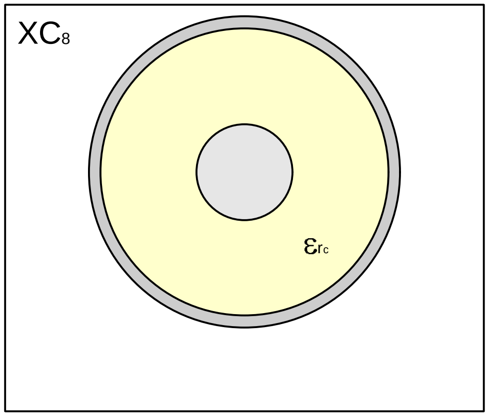


**Electric Fields**



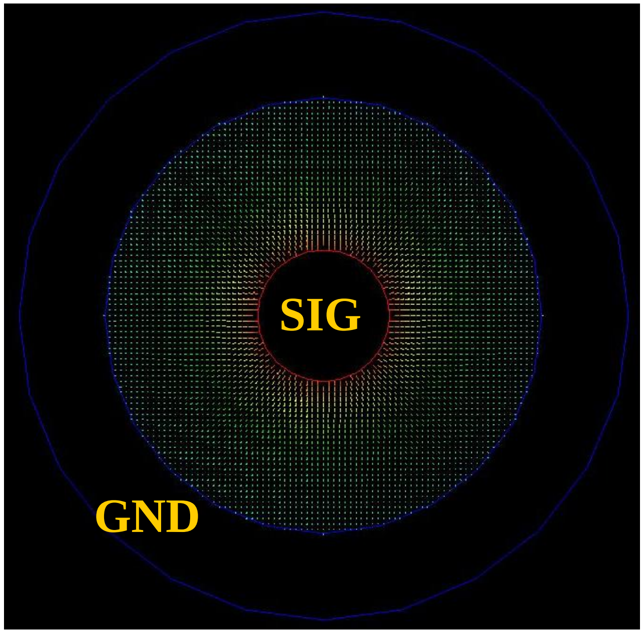
**Magnetic Fields**

# Modeling Results (XC8)

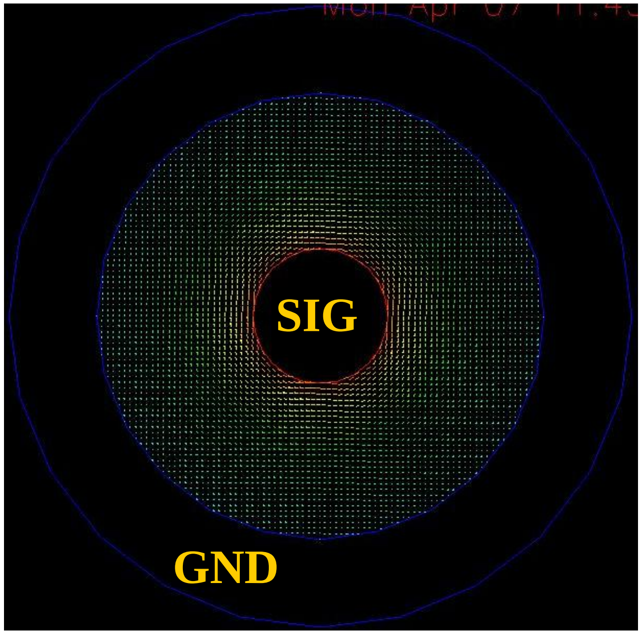


## Field Solver Results

$$Z_0 = 50 + j0$$
$$g = 0 + j296$$



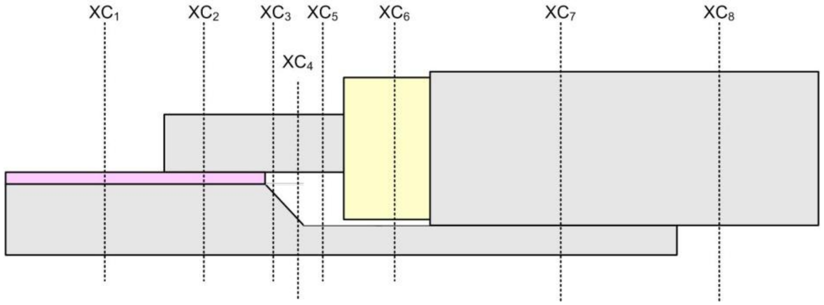
Electric Fields



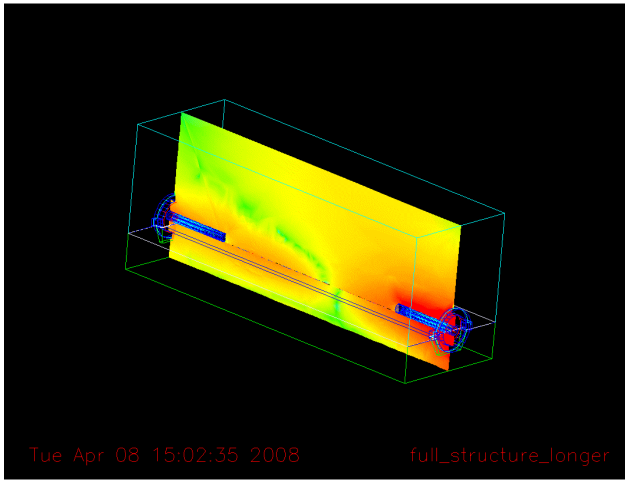
Magnetic Fields

# Modeling Results

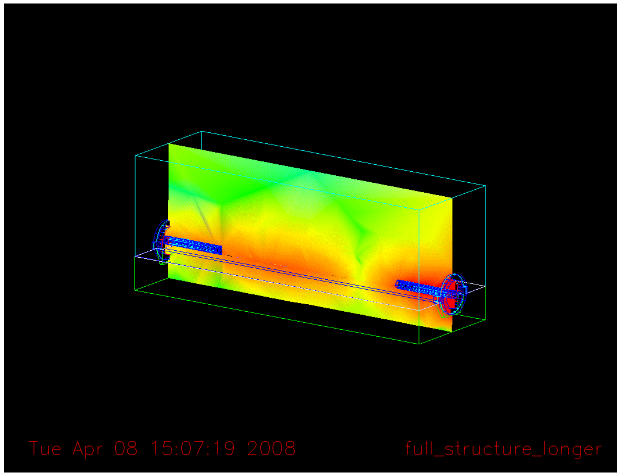
## Field Solver Results Summary



| Region | $Z_0$ | g |
|---|---|---|
| | | |
| XC1 | 52 + j26 | 305 + j615 |
| XC2 | 50 + j25 | 299 + j604 |
| XC3 | 114 + j3 | 10 + j269 |
| XC4 | 128 + j1 | 4 + j239 |
| XC5 | 134 + j1 | 3 + j229 |
| XC6 | 111 + j1 | 5 + j276 |
| XC7 | 50 + j0 | 0 + j296 |
| XC8 | 50 + j0 | 0 + j296 |



**Electric Fields**

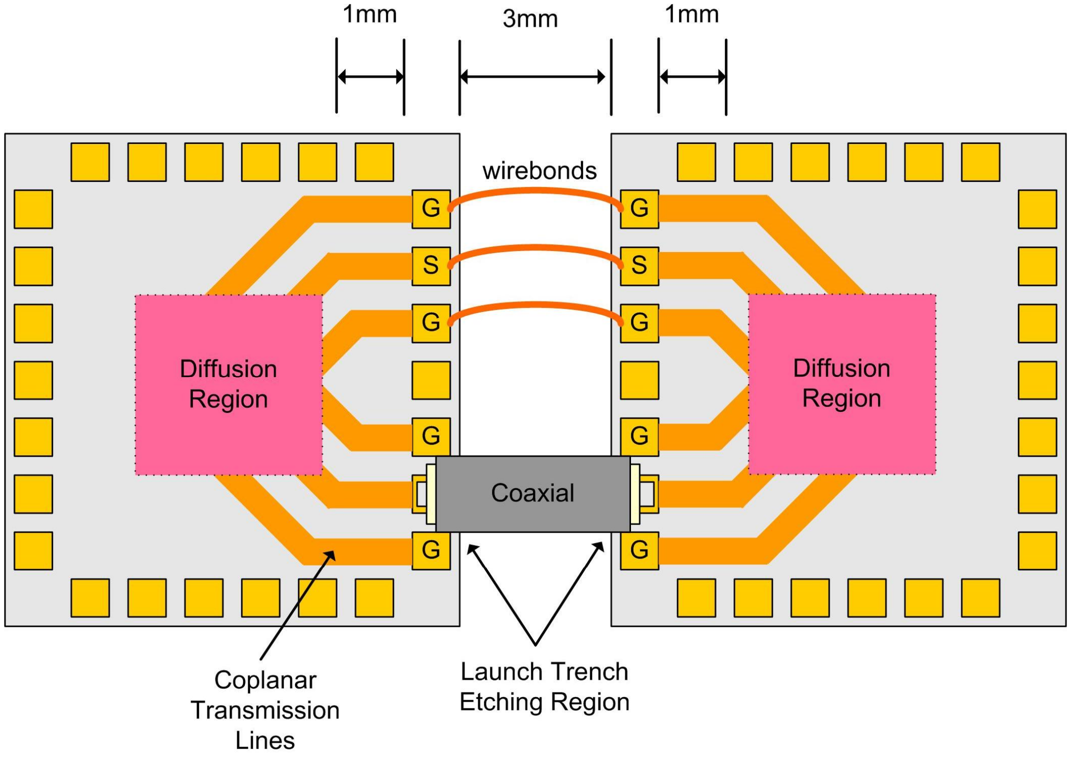


**Magnetic Fields**

# Electrical Evaluation (Comparison to Wirebond)

- Comparing to a chip-to-chip application where coplanar lines are used on-chip (35ps risetime)

Signal Path 1: Using a G/S/G wirebond interconnect structure
Signal Path 2: Using the new coaxial launch structure



# Spatial Evaluation

## Wire bond Comparison

- Is this interconnect comparable in size to that of the pads for wire bonding?

- We evaluate against 100µm x 100µm pad requirements for wire bond in G-S-G configuration with 100µm spacing

## Results

- Wire Bond Pads for G-S-G:

$$= 3*(W_{pad}) + 2*(W_{space})$$
$$= 3*(100\mu m) + 2*(100\mu m) = 500\ \mu m$$

- Coaxial Launch for G-S-G:

$$= W_{ttop} + 2*W_{gnd}$$
$$= 349\mu m + 2*100\ \mu m = 549\ \mu m$$

| Region | Parameter | Units | Coaxial Line | |
|---|---|---|---|---|
| | | | UT-013 | UT-020 |
| Coaxial Structure | $D_{oc}$ | µm | 330 | 584 |
| | $D_{od}$ | µm | 254 | 419 |
| | $D_{cc}$ | µm | 79 | 127 |
| Coplanar Structure | $T_{sig}$ | µm | 1 | 1 |
| | $T_{ox}$ | µm | 0.8 | 0.8 |
| | $W_{sig}$ | µm | 239 | 446 |
| | $W_{gnd}$ | µm | 100 | 100 |
| | $S_{copl}$ | µm | 55 | 90 |
| | $S_{ss}$ | µm | 634 | 916 |
| Trench Structure | $W_{ttop}$ | µm | 349 | 626 |
| | $W_{tbot}$ | µm | 150 | 228 |
| | $W_{tsw}$ | µm | 100 | 169 |
| | $H_{tsw}$ | µm | 141 | 239 |
| Transition Region | $L_{trench}$ | µm | 1100 | 1170 |
| | $L_{dext}$ | µm | 500 | 500 |
| | $L_{sw}$ | µm | 100 | 170 |
| | $L_{cext}$ | µm | 1000 | 1000 |
| | $L_{ccov}$ | µm | 900 | 831 |

**only 9.8% more area required**

# Electrical Evaluation (Parasitics)

## Electrical Evaluation

- Interconnect comparison
  - · Coax length = 3mm
  - · Wire bond length = 3mm

| Parameter | Units | Wire Bond | Coaxial Line |
|---|---|---|---|
| L' | nH/m | 569 | 242 |
| C' | pF/m | 26 | 97 |
| Zo | Ω | 148 | 50 |
| $L_{3mm}$ | nH | 1.71 | 0.73 |
| $C_{3mm}$ | pF | 0.08 | 0.29 |

## Results

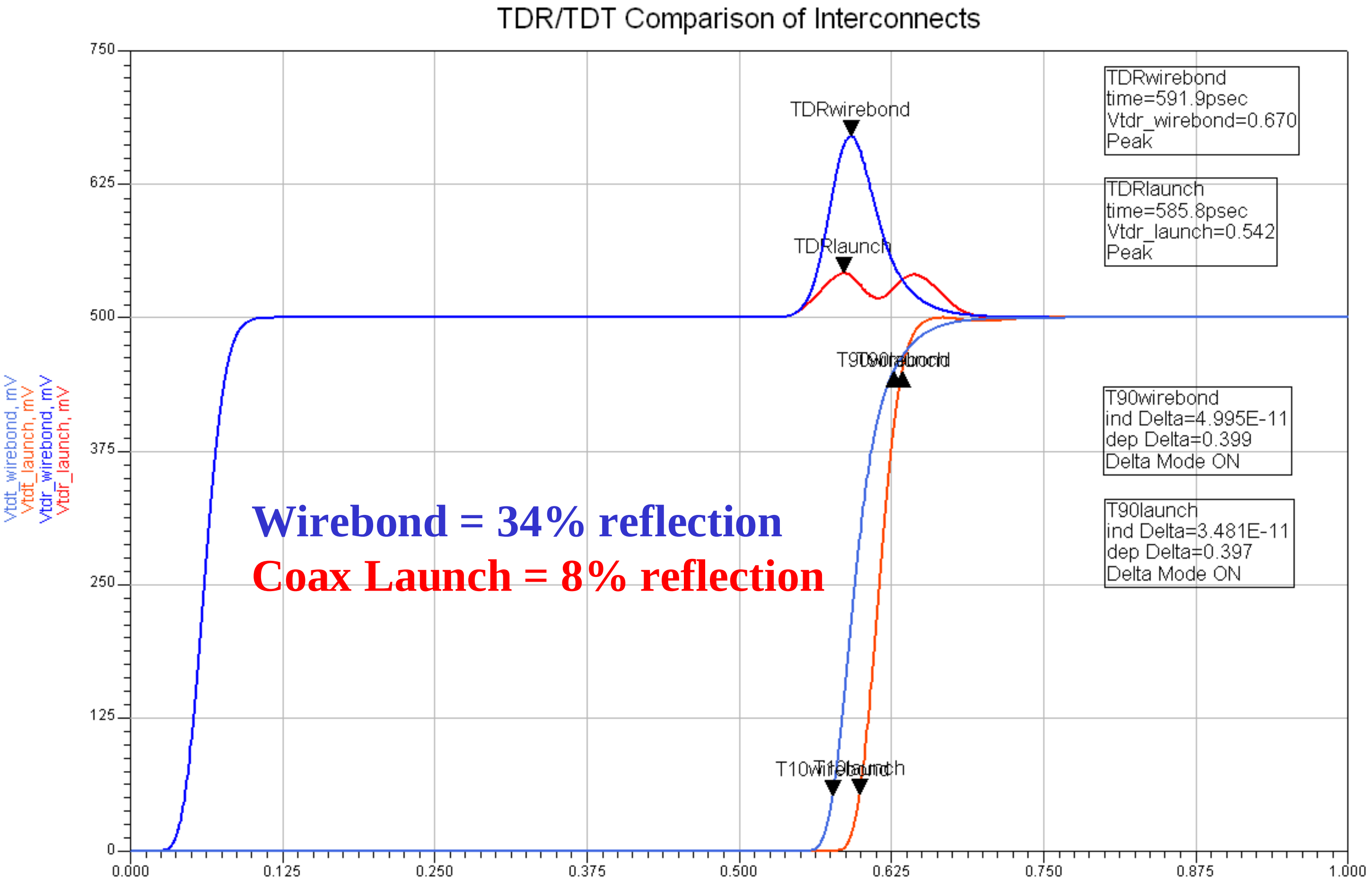
- Versus **wire bond**:

Inductance reduced **by 57%**

Impedance reduced **by 66%**

- Note: Interconnect is now ***Shielded*** and has ***Controlled Impedance***

# Electrical Evaluation (TDR/TDT)

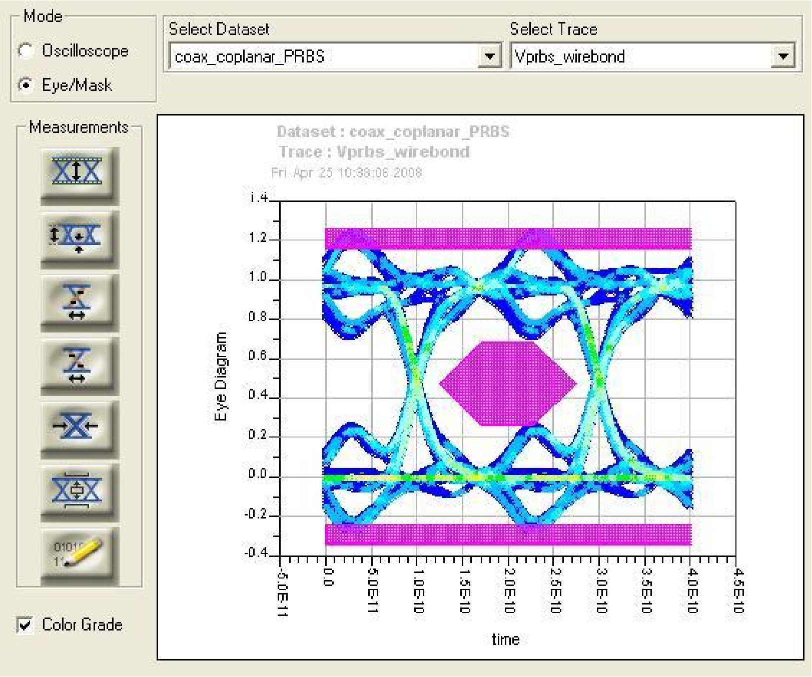


**Wirebond = 34% reflection**

**Coax Launch = 8% reflection**

# Electrical Evaluation (Eye Diagram)

## Eye Diagrams of a 5Gb/s, PRBS for a Load Terminated System



Mode
○ Oscilloscope
● Eye/Mask

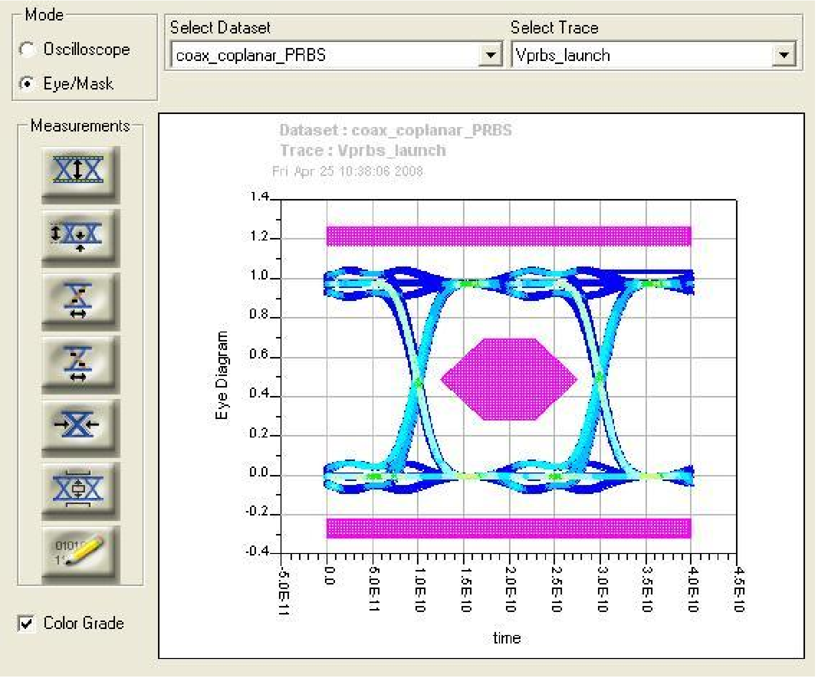
Select Dataset: coax_coplanar_PRBS

Select Trace: Vprbs_wirebond

☑ Color Grade

Dataset : coax_coplanar_PRBS
Trace : Vprbs_wirebond
Fri Apr 25 10:38:06 2008

**Wire bond**



Mode
○ Oscilloscope
● Eye/Mask

Select Dataset: coax_coplanar_PRBS

Select Trace: Vprbs_launch

☑ Color Grade

Dataset : coax_coplanar_PRBS
Trace : Vprbs_launch
Fri Apr 25 10:38:06 2008

**Coplanar to Coax**

# Summary

**1) A new SiP interconnect was presented and compared to current technology**

- Coaxial to Coplanar launch using MEMS trench
- Selective processing for high-speed nets

**2) Spatially this interconnect takes similar area requirements for G:S:G**

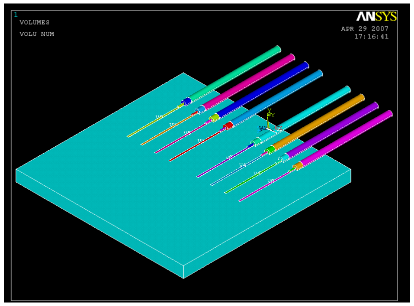
**3) Electrically this interconnect has the potential to perform faster**

- Controlled impedance reduces reflections
- Shielded interconnect eliminates signal coupling

**4) Next Steps**

- Fabrication underway at Montana State
- Measurements on prototypes expected during summer of 2008

# Questions?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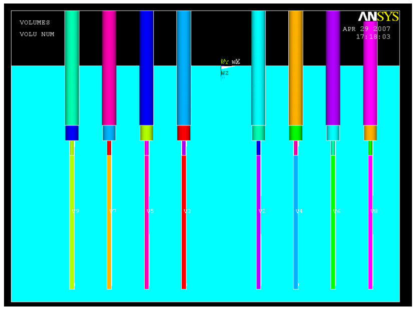
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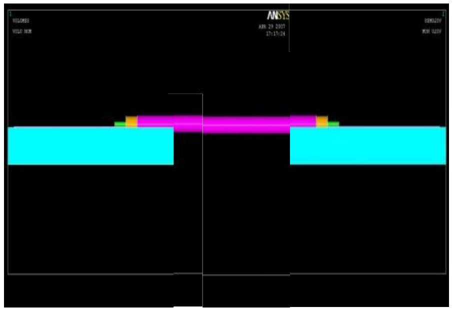
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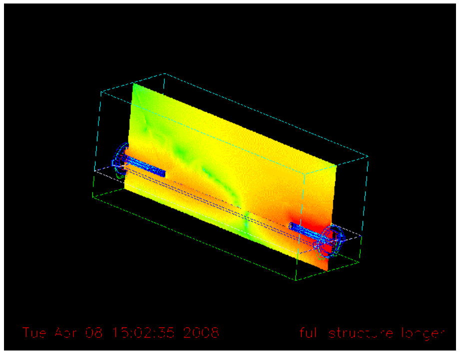
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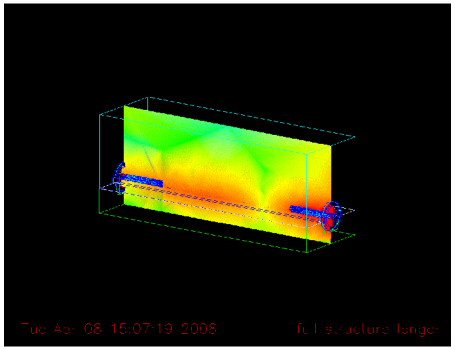
full structure longer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