EELE 261 – Introduction to Logic Circuits (4cr)
Department of Electrical & Computer Engineering
Montana State University - Bozeman, MT
Summer 2018 – 4x4 Session 2 - 6/11/18 to 7/6/18 - Fully Online

Description: This course introduces the concepts of classical digital logic design including number systems, interfacing, Boolean algebra, combinational logic design, and finite state machines. This course also covers Hardware Description Languages for the design and simulation of digital systems. Modern digital design of combinational logic and state machines is covered using VHDL and a logic synthesizer. This course contains a laboratory experience where students design and implement logic circuits using discrete parts and programmable logic devices.

Outcomes: At the end of this course a student should be able to:

1) Describe the differences between an analog and digital system,
2) Perform number system conversions and simple binary arithmetic,
3) Read logic circuit specifications and apply them to successfully interface digital circuits,
4) Synthesize, manipulate and minimize combinational logic circuits,
5) Describe the purpose and constructs of a hardware description languages,
6) Describe the operation of MSI logic circuits,
7) Synthesize finite state machine circuitry from a word description or state diagram,
8) Design and simulate combinational logic and finite state machines using VHDL,
9) Implement combinational logic and finite state machines using discrete parts,
10) Implement combinational logic and finite state machines on a programmable logic device using VHDL and a logic synthesizer.

Instructor: Dr. Brock J. LaMeres (call me Brock)
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Time & Location: 4 week summer session #2 (6/11/18 – 7/6/18), Fully Online

Required Material: This is a <u>fully online</u> course that will consist of reading and video assignments, working online homework problems, taking online quizzes/exams, and performing laboratory experiments using a portable kit. This course will use the *Brightspace D2L* course management system. All handouts, homework, quizzes/exams, and video content will be provided through Brightspace. Lab demo's will be conducted by uploading screenshots of measurements and short videos of your circuit operation. The following items are required for this course.

1) A computer with high speed internet running Windows. Our design software doesn't support Macs.

2) The textbook.

   Introduction to Logic Circuits and Logic Design with VHDL,
   Springer International Publishing, 1st Edition
   by Brock J. LaMeres
   (Hardcover ISBN 978-3-319-34194-1, eBook ISBN ISBN 978-3-319-34195-8)

   The hardcover version is available for purchase at the MSU bookstore. However, I suggest looking on amazon.com as I see it regularly on sale for $60 for a new version.

3) Digital logic portable lab kit. Kits are checked out and must be returned after course ends.

4) A camera capable of taking short videos of lab demos, usually just a smartphone.

Pre-Requisites: A course in algebra.

Course Website:	https://ecat1.montana.edu/ This is the *BrightSpace LE* course management system. This website will be used for all materials within the course. If you have technical difficulties with the system (i.e., can't login, the system is down, etc…), contact the Desire2Learn Help Desk at 994-3255.
Office Hours & Lab Demos:	The primary mode of communication with the instructor will be email. We can also have office hours using video conferencing through Google+ Hangout upon request. The hours that the instructor will be available each week will be determined after meeting with the class during the first week. Lab demos are handled via uploading short videos taken on your phone to Brightspace.
Grading Distribution:	Weekly Homework - 290 pts (29%) There will be 1000 points available Labs - 250 pts (25%) throughout the course. End of Module Quizzes - 210 pts (21%) Exam(s) - 250 pts (25%)
Grading Scale:	90% - 100%= A 80% - 89% = B 70% - 79% = C 60% - 69% = D 0% - 59% = F Note 1: The instructor reserves the right to apply a grading curve and to assign +/-'s to grades as appropriate. Note 2: A passing grade in the laboratory (>70%) component of this class is necessary to pass the course.
Academic Policies:	This course will follow the policies outlined in the *Conduct Guidelines and Grievance Procedures for Students" (http://www2.montana.edu/policy/student_conduct/)* and the *MSU Policy and Procedures Manual (http://www2.montana.edu/policy/)*) . Please consult these documents on policies regarding academic honesty, student and instructor rights, and general standards of conduct.
Course Components:	Reading: This course covers chapters 1-7 in the textbook. The course will follow the textbook EXACTLY. All homework, quiz, and exam problems are directly out of the book. Instructional Videos: There will be short videos for each section in the textbook and each lab. Homework **(graded, 290 pts)**: There will be weekly, graded homework. These will be in the form of either an online quiz within the D2L system or a VHDL simulation that will be uploaded to a Brightspace *Assignment* folder. You can open and work on the multiple choice homework for as long as you'd like as long as you submit before the deadline. Laboratory **(graded, 250 pts)**: There will be weekly laboratory exercises that will be conducted using the portable lab kit checked out from the instructor. Each lab will be demonstrated to the instructor by uploading screenshots of measurements or short videos (<5 seconds). End of Module Quizzes **(graded, 210 pts)**: There are 7 modules that will be covered in this course. The time spent on each module ranges between 1 to 3 weeks. At the end of each module there will be an end-of-module quiz. **Quizzes are TIMED**. Once you start, you have a predetermined about of time to complete and submit. The time allowed is based on how many weeks the module covered and range between 30 to 90 minutes. Exams **(graded, 250 pts)**: There will be a midterm exam and a final exam, each worth 125 points. These exams will be fully online. **Exams are TIMED**.